CLAIMS

What is claimed is:

1. An integrated circuit (IC) package substrate comprising a plurality of conductors within an IC mounting region, each conductor to be electrically coupled to a respective terminal of an IC, and at least one capacitor within the IC mounting region.

2. The IC package substrate recited in claim 1, wherein the at least one capacitor is electrically coupled to at least one conductor.

3. The IC package substrate recited in claim 2, wherein the at least one capacitor is mounted atop the at least one conductor.

4. The IC package substrate recited in claim 3, wherein the at least one capacitor is a capacitor array comprising two surfaces, each having a plurality of terminals of first and second polarity types.

5. The IC package substrate recited in claim 4, wherein the plurality of terminals of the capacitor array are disposed over substantially the entire surfaces.

6. The IC package substrate recited in claim 2, wherein the at least one capacitor is mounted beside the at least one conductor.

7. The IC package substrate recited in claim 1, wherein the conductors include at least one conductive bar having a height and a width, the height exceeding the width, and wherein the at least one capacitor is mounted beside and in electrical contact with the at least one conductive bar.

8. The IC package substrate recited in claim 1, wherein the plurality of conductors are substantially parallel to one another.

9. The IC package substrate recited in claim 8, wherein the at least one capacitor is non-orthogonally mounted atop the at least one conductor.

10. The IC package substrate recited in claim 1 and comprising a plurality of capacitors distributed substantially throughout the IC mounting region, each capacitor being in electrical contact with at least one of the conductors.

11. The IC package substrate recited in claim 10, wherein the plurality of capacitors comprises a plurality of sets of capacitors, each set comprising one or more capacitors aligned substantially end-to-end.

12. The IC package substrate recited in claim 1, wherein the conductors include pads.

13. An integrated circuit (IC) comprising:

a plurality of conductive bars on a surface of the IC, each conductive bar to be electrically coupled to a respective terminal of an IC package substrate; and

at least one capacitor having terminals coupled to at least two of the conductive bars.

14. The IC recited in claim 13, wherein the conductive bars have a height and a width, the height exceeding the width.

15. The IC recited in claim 14, wherein the at least one capacitor is mounted beside and in electrical contact with the at least two conductive bars.

16. An integrated circuit (IC) package comprising:

a substrate having a plurality of conductors within an IC mounting region;

at least one capacitor within the IC mounting region and electrically coupled to at least one of the conductors; and

an IC electrically coupled to the plurality of conductors.

17. The IC package recited in claim 16, wherein the at least one capacitor is electrically coupled to first and second conductors of the plurality of conductors, and wherein the first conductor is to couple to a first potential, and the second conductor is to couple to a second potential.

18. The IC package recited in claim 16, wherein the at least one capacitor is mounted atop the at least one conductor.

19. The IC package recited in claim 18, wherein the at least one capacitor is mounted atop two conductors.

20. The IC package recited in claim 18, wherein the at least one capacitor is an capacitor array having two surfaces, each having a plurality of terminals of first and second polarity types.

21. The IC package recited in claim 20, wherein the plurality of terminals are disposed over substantially the entire surfaces.

22. The IC package recited in claim 16, wherein the at least one capacitor is mounted beside the at least one conductor.

23. The IC package recited in claim 16, wherein the at least one capacitor is mounted between two conductors.

24. The IC package recited in claim 16, wherein the at least one capacitor has a top, a bottom, and a pair of opposing sides, and wherein the at least one capacitor is

from the group comprising a capacitor having terminals on its top and bottom, a capacitor having terminals on its opposing sides, and a capacitor having terminals on its top, bottom, and opposing sides.

25. The IC package recited in claim 16, wherein the conductors include at least one conductive bar having a height and a width, the height exceeding the width, and wherein the at least one capacitor is mounted beside and in electrical contact with the at least one conductive bar.

26. The IC package recited in claim 16, wherein the plurality of conductors are substantially parallel to one another.

27. The IC package recited in claim 26, wherein the at least one capacitor is non-orthogonally mounted atop the at least one conductor.

28. The IC package recited in claim 16 and comprising a plurality of capacitors distributed substantially throughout the IC mounting region, each capacitor being in electrical contact with at least one of the conductors.

29. The IC package recited in claim 28, wherein the plurality of capacitors comprises a plurality of sets of capacitors, each set comprising one or more capacitors aligned substantially end-to-end.

30. The IC package recited in claim 16, wherein the conductors include pads.

31. An electronic assembly comprising:
a printed circuit board (PCB); and
an integrated circuit (IC) package coupled to the PCB and including
a substrate having a plurality of conductors within an IC mounting region;

at least one capacitor within the IC mounting region and electrically coupled to at least one of the conductors; and

an IC electrically coupled to the plurality of conductors.

32. The electronic assembly recited in claim 31, wherein the at least one capacitor is electrically coupled to two of the conductors, one conductor to couple to a first potential, the other conductor to couple to a second potential.

33. The electronic assembly recited in claim 31, wherein the at least one capacitor is mounted atop the at least one conductor.

34. The electronic assembly recited in claim 31, wherein the at least one capacitor is mounted beside the at least one conductor.

35. An electronic system comprising:

a bus coupling components in the electronic system;

a display coupled to the bus;

external memory coupled to the bus; and

a processor coupled to the bus and comprising an electronic assembly including:

a printed circuit board (PCB); and

an integrated circuit (IC) package coupled to the PCB and including

a substrate having a plurality of conductors within an IC mounting region;

at least one capacitor within the IC mounting region and electrically coupled to at least one of the conductors; and

an IC electrically coupled to the plurality of conductors.

36. The electronic system recited in claim 35, wherein the at least one capacitor is mounted atop the at least one conductor.

37. The electronic system recited in claim 35, wherein the at least one capacitor is mounted beside the at least one conductor.

38. A method of fabricating an IC package substrate comprising:

arranging a plurality of capacitors on a surface of an integrated circuit (IC) package substrate within an IC mounting region thereof; and

securing the plurality of capacitors to the surface.

39. The method recited in claim 38, wherein the surface comprises a plurality of conductors, wherein each capacitor comprises terminals of first and second polarity types, and wherein, in arranging, the plurality of capacitors are disposed such that terminals of the first polarity type contact a first set of the plurality of conductors, and terminals of the second polarity type contact a second set of the plurality of conductors.

40. The method recited in claim 38, wherein, in securing, a fill material is applied to the plurality of capacitors and to openings between the capacitors.

41. A method comprising:

forming at least one capacitor assembly, the at least one capacitor assembly having at least one capacitor electrically coupled to a conductor; and

mounting the at least one capacitor assembly to a surface of an integrated circuit (IC) package substrate within an IC mounting region thereof.

42. The method recited in claim 41, wherein the conductor comprises a conductive bar having a height and a width, the height exceeding the width.

43. The method recited in claim 41 and further comprising:

applying a fill material to the at least one capacitor assembly.

44. A method comprising:

arranging a plurality of capacitors within an IC mounting region on a surface of an integrated circuit (IC) package substrate; and

mounting an IC on the mounting region.

45. The method recited in claim 44, wherein, in arranging, the plurality of capacitors are coupled to electrical conductors within the IC mounting region.

46. The method recited in claim 45, wherein the IC has a plurality of terminals, and wherein, in arranging, at least one capacitor of the plurality of capacitors is coupled between a respective IC terminal and a respective electrical conductor within the IC mounting region.

47. The method recited in claim 44, wherein, in arranging, the plurality of capacitors are coupled to electrical conductors within the IC mounting region, the electrical conductors including a plurality of conductive bars each having a height and a width, the height exceeding the width.

48. The method recited in claim 47, wherein, in arranging, at least one capacitor of the plurality of capacitors is coupled between adjacent ones of the plurality of conductive bars.

49. The method recited in claim 44, wherein, in mounting, the IC is electrically coupled to the plurality of capacitors.

50. A method comprising:

placing a capacitor array within an IC mounting region on a surface of an integrated circuit (IC) package substrate; and

mounting an IC on the mounting region.

51. The method recited in claim 50, wherein the capacitor array has a plurality of terminals, and wherein, in placing, the plurality of terminals of the capacitor array are coupled to respective conductors within the IC mounting region.

52. The method recited in claim 51, wherein the IC has a plurality of terminals, and wherein, in mounting, the plurality of terminals of the IC are coupled to respective ones of the plurality of terminals of the capacitor array.

53. A method comprising:

forming at least one capacitor assembly, the at least one capacitor assembly having at least one capacitor electrically coupled to a conductor; and

mounting the at least one capacitor assembly to a surface of an integrated circuit (IC).

54. The method recited in claim 53, wherein the conductor comprises a conductive bar having a height and a width, the height exceeding the width.

55. The method recited in claim 53 and further comprising:

applying a fill material to the at least one capacitor assembly.

56. A method comprising:

arranging a plurality of capacitors on a surface of an integrated circuit (IC); and

mounting the IC on a mounting region of an IC package substrate.

57. The method recited in claim 56, wherein, in arranging, the plurality of capacitors are coupled to electrical conductors on the IC surface.

58. The method recited in claim 57, wherein the IC package substrate has a plurality of terminals, and wherein, in arranging, at least one capacitor of the plurality of capacitors is coupled between a respective IC package substrate terminal and a respective electrical conductor on the IC surface.

59. The method recited in claim 56, wherein, in arranging, the plurality of capacitors are coupled to electrical conductors on the IC surface, the electrical conductors including a plurality of conductive bars each having a height and a width, the height exceeding the width.

60. The method recited in claim 59, wherein, in arranging, at least one capacitor of the plurality of capacitors is coupled between adjacent ones of the plurality of conductive bars.

61. The method recited in claim 56, wherein, in mounting, the IC package substrate is electrically coupled to the plurality of capacitors.

62. A method comprising:

forming a first set of conductive bars on a surface of an integrated circuit (IC) package substrate;

forming a second set of conductive bars on a surface of an IC;

affixing at least one capacitor to at least two conductive bars from the group comprising the first and second sets of conductive bars; and

mounting the IC on an IC mounting region of the IC package substrate.

63. The method recited in claim 62, wherein, in forming, the conductive bars have a height and a width, the height exceeding the width, and wherein the height of the first set of conductive bars is substantially identical to the height of the second set of conductive bars.

64. The method recited in claim 63, wherein, in forming, the height of the first set of conductive bars is substantially different from the height of the second set of conductive bars, and wherein, in mounting, bars from the first set of conductive bars are coupled to bars from the second set of conductive bars to form conductive bars having a final height.